IN THE SPECIFICATION

Please replace the paragraph beginning at page 2, line 7 with the following rewritten paragraph:

Then, after depositing a second inter-insulation layer 140 on the first inter-insulation layer 120, bitline ~~contacts~~ contact holes 145 are formed to expose corresponding ones of the contact pads 130, that is, the corresponding contact pads that are to be connected with bitlines in a subsequent process.

Please replace the paragraph beginning at page 2, line 11 with the following rewritten paragraph:

After depositing a metal film for a contact pad, for example, a tungsten film on the entire surface of the substrate including the bitline ~~contacts~~ contact holes 145, the tungsten film is etched by a chemical-mechanical polishing process (CMP) or an etch back process, thereby forming bitline contact pads 150 in the bitline ~~contacts~~ contact holes 145.

Please replace the paragraph beginning at page 2, line 15 with the following rewritten paragraph:

Referring to FIG. 2B and FIG. 3B, a conductive material 161 for a bitline, such as a tungsten film, and the bitline capping layer 165, such as a silicon nitride film, are sequentially deposited on the second inter-insulation layer 140 and patterned to form bitlines 160. Each bitline includes the stacked conductive material 161 and the capping layer 165. The bitline 160 is electrically connected to the bitline contact pad 150 formed in the bitline ~~contacts~~ contact holes 145. An insulating film, such as a silicon nitride film, for a bitline spacer is deposited on the second inter-insulation layer 140 including the bitlines 160 and etched to form bitline spacers 170.

Please replace the paragraph beginning at page 2, line 23 with the following rewritten paragraph:

Referring to FIG. 2C and FIG. 3C, a third inter-insulation layer 180 is formed on a second inter-insulation layer 140 including the bitlines 160. By etching the second and the third inter-insulation layers 140 and 180, storage node ~~contacts~~ contact holes 185 are formed to expose corresponding contact pads of the contact pads 130, that is, the corresponding contact pads connected to the storage node contact pads to be formed in a subsequent process.

Please replace the paragraph beginning at page 2, line 28 with the following rewritten paragraph:

After depositing a poly-silicon film on the third inter-insulation layer 180 to fill the storage node contacts 185, storage node contact pads 190 are formed through a CMP method and others. The storage node contact pad 190 is electrically connected to the contact pad 130 through the storage node ~~contacts~~ contact holes 185. Then, storage nodes 200 of capacitors connected to the storage node contact pads 190 are formed.

Please replace the paragraph beginning at page 3, line 7 with the following rewritten paragraph:

To solve the above problems of the prior art, a method of forming bitlines through a damascene process has been suggested. When forming bitlines of a semiconductor device having a COB structure with a damascene process, it is necessary to surround the bitlines by forming materials having etching selectivity with an inter-insulation layer of an oxide film, for instance, a capping layer and a spacer comprised of a silicon nitride film on tops and side walls of the bitlines, in order to protect the bitlines during the next process of forming a storage node contact hole.

Please replace the paragraph beginning at page 3, line 14 with the following rewritten paragraph:

A technology of protecting the bitlines by perfectly surrounding a damascene bitline with the capping layer and the spacer has been suggested in Korean Patent Laid Open Report No. 2001-55685. The above technology forms a bitline that is perfectly surrounded by a spacer comprised of a silicon nitride film, thereby obtaining process margins by protecting the bitlines during the storage node contact hole process. However, it causes the increase of parasitic capacitance since a silicon nitride film between neighboring bitlines has a higher dielectric constant than an oxide film.

Please replace the paragraph beginning at page 3, line 24 with the following rewritten paragraph:

Embodiments of the invention provide a semiconductor device and a fabrication method thereof for improving process margins while forming a storage node contact hole by forming a stud type bitline capping layer.

Please replace the paragraph beginning at page 3, line 27 with the following rewritten paragraph:

Embodiments of the invention also provide a semiconductor device and a fabricating method thereof for reducing parasitic capacitance between bitlines and between a bitline and a storage node contact hole by surrounding the bitline with an oxide film.

Please replace the paragraph beginning at page 5, line 26 with the following rewritten paragraph:

Referring to FIG.5B, FIG.6B, and FIG.7B, bitline ~~contacts~~ contact holes 345 and bitline patterns 355 are formed by etching the second inter-insulation layer 340 through a dual damascene process. At this time, the bitline ~~contacts~~ contact holes 345 are formed to expose corresponding contact pads of the contact pads 330, that is, the corresponding contact pads connected to bitlines that will be formed in a subsequent process. The bitline patterns 355 are formed to cross with the gates and have a grooved shape.

Please replace the paragraph beginning at page 5, line 32 with the following rewritten paragraph:

When forming the bitline ~~contacts~~ contact holes 345 and the bitline patterns 355 by etching the second inter-insulation layer 340 through the dual damascene process, it is possible to form the bitline patterns 355 after forming the bitline ~~contacts~~ contact holes 345 or form the bitline ~~contacts~~ contact holes 345 after forming the bitline patterns 355. At this point, the bitline ~~contacts~~ contact holes 345 are formed by etching the second inter-insulation layer 340, using the contact pads 330 as an etching stop film.

Please replace the paragraph beginning at page 6, line 5 with the following rewritten paragraph:

Referring to FIG.5C, FIG.6C and FIG.7C, a conductive material 361 for a bitline, such as a tungsten film, is deposited on the second inter-insulation layer 340 including bitline ~~contacts~~ contact holes 345 and bitline patterns 355. Referring to FIG.5D, FIG.6D and FIG.7D, the conductive material 361 is over-etched to be left in the bitline ~~contacts~~ contact holes 345 and a portion of the bitline patterns 355.

Please replace the paragraph beginning at page 6, line 15 with the following rewritten paragraph:

In an embodiment of the present invention, the bitline ~~contacts~~ contact holes 345 are also filled when the bitline patterns 355 are filled with the conductive material 361 for a bitline, rather than filling the bitline patterns 355 with the conductive material 361 for a bitline after forming contact plugs in the bitline ~~contacts~~ contact holes 345 through another process.

Please replace the paragraph beginning at page 7, line 20 with the following rewritten paragraph:

On this occasion, only half the thickness of the second capping material 365 is surrounded by the second inter-insulation 340, so that it can obtain process margins as well as maintain insulating properties and reduce parasitic capacitance between bitlines 360 and between a bitline 360 and a storage node contact hole in a subsequent process.

Please replace the paragraph beginning at page 7, line 21 with the following rewritten paragraph:

Referring to FIG.5H, FIG.6H, and FIG.7H, a third inter-insulation layer 370 of an oxide film series is deposited on the entire surface of the substrate and the second and the third inter-insulation layers 340 and 370 are etched to form storage node ~~contacts~~ contact holes 375. The storage node ~~contacts~~ contact holes 375 expose corresponding contact pads of the contact pads 330 that are connected with storage nodes to be formed in a subsequent process. The second and the third inter-insulation layers 340 and 370 are self align-etched with the spacer 367 of the bitline capping layer 369 serving as an etching stop layer, thereby forming the self-aligned storage node contact ~~contacts~~ contact holes 375.

Please replace the paragraph beginning at page 7, line 32 with the following rewritten paragraph:

Referring to FIG.5I, FIG.6I, FIG.7I, a conductive material such as a poly-silicon film is deposited on the third inter-insulation layer 370 including the storage node contact hole 375 and is smoothed through a CMP or an etch back process, thereby forming storage node contact plugs 380. Subsequently, storage nodes 390 for capacitors electrically connected with the storage node contact plugs 380 are formed.

Please replace the paragraph beginning at page 8, line 3 with the following rewritten paragraph:

As shown above, with a method of fabricating a semiconductor device in accordance with an embodiment of the invention, the storage node contact hole 375 is self align-etched and sufficient etching process margin is ensured. By forming a stud-shaped bitline capping layer, the capping layer serves as an etching stop layer during an etching process for forming the storage node contact hole. In addition, the second and the third inter-insulation layers 340 and 370 with an oxide film series having a lower dielectric constant than a silicon nitride film exist between adjacent bitlines 360 and between the bitline 360 and the storage node contact plug 380, reducing the parasitic capacitance between them.

Please replace the paragraph beginning at page 8, line 11 with the following rewritten paragraph:

FIG.11A is a diagram illustrating the relationship between the thickness of a bitline capping layer and the parasitic capacitance. It is found that a reduced threshold value of the parasitic capacitance occurs when the thickness of the silicon nitride bitline capping layer is about 1000Å. FIG. 11B is a diagram illustrating the relationship between the compositions of a bitline spacer and the parasitic capacitance. 'A' shows the distribution of the parasitic capacitance in the case where the bitline spacer is fully composed of an oxide film, while 'C' shows the distribution of the parasitic capacitance in the case where the bitline spacer is fully composed of a silicon nitride film. 'B' shows the distribution of the parasitic capacitance in the case where the bitline spacer is partially comprised of an oxide film, that is, in the case where an oxide film exists between the bitlines and a silicon nitride film exists between the bitline and the storage node contact hole. Referring to FIG.11B, it is found that the parasitic capacitance is reduced by 30% and 40%, respectively, in case A and case B as compared to the case C where the bitline spacer is fully composed of a silicon nitride film.

Please replace the paragraph beginning at page 8, line 24 with the following rewritten paragraph:

Seeing FIG.11A and FIG.11B, the invention can minimize the parasitic capacitance as well as maintain insulating properties and also improve process margins for forming a storage node contact hole by forming a stud-shaped bitline capping layer.

Please replace the paragraph beginning on page 8, line 32, with the following rewritten paragraph:

A method of fabricating a semiconductor device in accordance with another embodiment of the invention is the same in some respects as the ~~methof~~ method of the previous embodiment. However, it is different in terms of forming a second inter-layer insulation layer with a stack structure where an upper oxide film, a lower oxide film, and a silicon nitride film for an etching stop layer are sandwiched between the upper oxide film and the lower oxide film. This is done in order to obtain etching stability in an etching process for forming the capping spacer.

Please replace the paragraph beginning at page 9, line 24 with the following rewritten paragraph:

Referring to FIG.8B, FIG.9B, and FIG.10B, bitline ~~contacts~~ contact holes 545 and bitline patterns 555 having a grooved shape are formed by etching the second inter-insulation layer 550 through a dual damascene process. At this moment, when etching the second inter-insulation layer 550, it should be etched without any etching selectivity between the upper and lower oxide films 551 and 553 and a silicon nitride film 552.

Please replace the paragraph beginning at page 9, line 29 with the following rewritten paragraph:

While forming the bitline contact hole 545 and the bitline pattern 555 through the dual damascene process, it is possible to form the bitline pattern 555 after forming the bitline contact hole 545, or to form the bitline contact hole 545 after forming the bitline pattern 555. On this occasion, when forming the bitline contact hole 545, the contact pad 530 serves as an etching stop film.

Please replace the paragraph beginning at page 10, line 33 with the following rewritten paragraph:

Though not shown in the drawings, after depositing a third inter-insulation layer, storage node ~~contacts~~ contact holes are formed by etching the third inter-insulation layer and the lower oxide film 551, and storage contact plugs are formed in the storage node contacts, and then storage nodes of capacitors electrically connected with the contact plugs are formed.

Please replace the paragraph beginning at page 11, line 6 with the following rewritten paragraph:

According to the embodiments of the invention described above, sufficient process margins can be obtained while forming a storage node contact hole by forming stud-type bitline capping layers, as well as reducing contact resistance by increasing the contact open regions. In addition, embodiments of the invention may decrease parasitic capacitance, since an oxide film having a lower dielectric constant than a silicon nitride film exists between adjacent bitlines and between a bitline and a storage node contact hole.

Please replace the paragraph beginning at page 11, line 13 with the following rewritten paragraph:

An embodiment of the invention provides a semiconductor device that includes an insulating film formed on a semiconductor substrate and having a bitline contact hole and a groove-shaped bitline pattern, a bitline formed on the bitline contact hole and in a portion of the bitline pattern and surrounded by the insulating film, and a bitline capping layer formed on the bitline within the bitline pattern and the insulating film. The bitline capping layer protrudes from the insulating film, and the protruded portion of the bitline capping layer is wider than a width of the bitline.

Please replace the paragraph beginning at page 11, line 25 with the following rewritten paragraph:

In addition, an embodiment of the invention provides a method of fabricating a semiconductor device that includes the processes of forming an insulating film on a semiconductor substrate, etching the insulating film to form a bitline contact hole and a groove-shaped bitline pattern, forming a bitline on the bitline contact hole and a portion of the bitline pattern, and forming a bitline capping layer on the bitline within the bitline pattern and on the insulating film that protrudes from the insulating film. The protruded portion of the bitline capping layer is wider than a width of the bitline.

Please replace the paragraph beginning at page 12, line 13 with the following rewritten paragraph:

Furthermore, embodiments of the invention provide a method of fabricating a semiconductor device that include the processes of forming a first insulating film having a bitline contact pad and a storage node contact pad on a semiconductor substrate, forming a

second insulating film on an entire surface of the substrate, etching the second insulating film to form a bitline contact exposing the bitline contact pad and a groove-shaped bitline pattern, forming a bitline in a portion of the bitline pattern that will be connected with the bitline contact pad through the bitline contact hole, forming a bitline capping layer on the bitline within the bitline pattern and the insulating film that protrudes from the second insulating film so that the protruded portion is wider than a width of the bitline pattern, forming a third insulating film on an entire surface of the substrate, and etching the second and the third insulating films to form a storage node contact hole that exposes the storage node contact pad.

Please replace the paragraph beginning at page 12, line 24 with the following rewritten paragraph:

The bitline contact hole and the bitline pattern are formed by using a dual damascene process, and after forming the bitline contact hole by etching the second insulating film using the bitline contact pad as an etching stop film, the bitline pattern is formed by etching the second insulating film. Alternatively, after forming the bitline pattern by etching the second insulating film, the bitline contact hole is formed by etching the second insulating film using the bitline contact pad as an etching stop film.